

ABSTRACT

A ferroelectric or high dielectric constant capacitor having a multilayer lower electrode comprising at least two layers – a platinum layer and a platinum-rhodium layer – for use in a random access memory (RAM) cell. The platinum layer of the lower electrode adjoins the capacitor dielectric, which is a ferroelectric or high dielectric constant dielectric such as BST, PZT, SBT or tantalum pentoxide. The platinum-rhodium layer serves as an oxidation barrier and may also act as an adhesion layer for preventing separation of the lower electrode from the substrate, thereby improving capacitor performance. The multilayer electrode may have titanium and/or titanium nitride layers under the platinum-rhodium layer for certain applications. The capacitor has an upper electrode which may be a conventional electrode or which may have a multilayer structure similar to that of the lower electrode. Processes for manufacturing the multilayer lower electrode and the capacitor are also disclosed.

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